

Abstract of the Disclosure

An integrated circuit carries an intellectual property core. The intellectual property core includes a test access
5 port 39 with test data input leads 15, test data output leads 13, control leads 17 and an external register present, ERP lead 37. A scan register 25 encompasses the intellectual property core and ERP lead 37 carries a signal indicating the presence of the scan register.

10

Fig. 3